ABSTRACT OF THE DISCLOSURE

A high-speed bit stream interface module interfaces a high-speed communication media to a communication Application Specific Integrated Circuit (ASIC) via a Printed Circuit Board (PCB) or the communication ASIC to another communication ASIC. The high-speed bit stream interface includes a line side interface, a board side interface, and a plurality of signal conditioning circuits. The signal conditioning circuits service each of an RX path and a TX path and include a limiting amplifier and a clock and data recovery circuit. The signal conditioning circuit may also include an equalizer and/or an output pre-emphasis circuit. The clock and data recovery circuit has an adjustable Phase Locked Loop (PLL) bandwidth that is set to correspond to a jitter bandwidth of a serviced high-speed bit stream.